10-19-06 10/724028 CJC

Docket No.: 08211/0200253-US0
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Letters Patent of:
Timothy Lance Blankenship et al.

Patent No.: 7,053,658

Issued: May 30, 2006

For: APPARATUS FOR CIRCUIT WITH KEEPER

Certificate
OCT 23 2006
of Correction

REQUEST FOR CERTIFICATE OF CORRECTION
PURSUANT TO 37 CFR 1.322

Attention: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Upon reviewing the above-identified patent, Patentee noted several Patent Office errors which should be corrected.

In the Specification:

Column 3, Line 66, Delete "MIO" and insert -- M10 --.

Column 4, Line 2, Delete "MIO" and insert -- M10 --.

The errors were not in the application as filed by applicant; accordingly no fee is required. Enclosed please find marked up copies of the specification.

OCT 24 2006

{S:\08211\0200253US0\00883128.DOC }

Transmitted herewith is a proposed Certificate of Correction effecting such amendment. Patentee respectfully solicits the granting of the requested Certificate of Correction.

Dated: October 16, 2006

Respectfully submitted,

By _____
Flynn Barrison
Registration No.: 53,970
DARBY & DARBY P.C.
P.O. Box 5257
New York, New York 10150-5257
(212) 527-7700
(212) 527-7701 (Fax)
Attorneys/Agents For Applicant

PTO/SB/44 (04-05)
Approved for use through 04/30/2007. OMB 0651-0033
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO.	:	7,053,658
APPLICATION NO.	:	10/724,028
ISSUE DATE	:	May 30, 2006
INVENTOR(S)	:	Timothy Lance Blankenship et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Specification:

Column 3, Line 66, Delete "MIO" and insert -- M10 --.

Column 4, Line 2, Delete "MIO" and insert -- M10 --.

{S:\08211\0200253US0\00883135.DOC }MAILING ADDRESS OF SENDER:
Flynn Barrison
DARBY & DARBY P.C.
P.O. Box 5257
New York, New York 10150-5257

OCT 24 2006

Figure 4 illustrates a schematic diagram of a circuit (400) that is another exemplary implementation of Figure 1. Circuit 400 is substantially similar to circuit 300 in some ways, albeit different in other ways. In circuit 400, keeper switch circuit 102 is implemented by transistor M9. Transistor M9 has a gate that is coupled to node N1, a drain that is coupled to node N13, and a source that is coupled to node N3.

Transistor M9 is configured to ensure that signal lr is actively driven independent of the voltage associated with signals in_hr and in_lr, including at the initial power-on state. Transistors M3 and M9 are n-type transistors.

Figure 5 illustrates a schematic diagram of a level-shifter circuit (500). Circuit 500 includes transistors M2-M5 and M11-M16, keeper circuit 102 (transistor M8) and another keeper circuit (transistor M10). Transistor M4 has a gate that is coupled to node N11, a drain that is coupled to a first complement output node N21, and a source that is coupled to a second complement output node N22. Transistor M10 has a gate that is coupled to node N21, a source that is coupled to node N22, and a drain that is coupled to node N11.

Transistor M8 is configured to operate in a substantially similar manner as described with regard to Figure 3, albeit different in some ways. Transistor M4 is arranged to operate as a cascode transistor in cooperation with transistor M12. Transistor M5 is configured to operate as a cascode transistor in cooperation with transistor M14. Circuit 500 is configured to provide signals hr, fr, lr, hrb, frb, and lrb in response to a data input signal (din). Signal hrb is a complement of signal hr, signal frb is a complement of signal fr, and signal lrb is a complement of signal lr. As an example, transistors M2, M4, M8, and M10 are each p-type transistors. Transistor M8 is configured to ensure that signal hr is actively driven regardless of the voltage associated with signal din. Transistor M10 is configured to ensure that signal hrb is actively driven regardless of the voltage associated with signal din.

Figure 6 illustrates a schematic diagram of a circuit (600) that is substantially similar to circuit 500, albeit different in some ways. In this embodiment, the keeper circuit 102 is implemented by transistor M9, and the other keeper circuit is implemented by transistor M17. In this example, transistors M3, M5, M9, and M17 are n-type

Application No. (if known): 10/724,028 Attorney Docket No.: 08211/0200253-US0

Certificate of Express Mailing Under 37 CFR 1.10

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail, Airbill No. in an envelope addressed to:

EV834732275-US

Attention: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

on October 17, 2006
Date

Signature

D. B. Peck

Typed or printed name of person signing Certificate

Registration Number, if applicable

Telephone Number

Note: Each paper must have its own certificate of mailing, or this certificate must identify each submitted paper.

Certificate of Correction (1 page)
Request for Certificate of Correction (2 pages)
Copy of the Specification (1 page)
Return Postcard